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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/502,675	02/11/00	YAMAZAKI	S 0756-2101

EXAMINER	
PERT, F	
ART UNIT	**PAPER NUMBER**
2813	11

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MM41/0913

DATE MAILED: 09/13/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No.	Applicant(s)	
	09/502,675	Yamazaki et al.	
	Examiner	Art Unit	
	Evan T. Pert	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 June 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-85* is/are pending in the application.

4a) Of the above claim(s) *45-79* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-44 and 80-85* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *5,7,8* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Election/Restrictions

1. Claims 45-79 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a non-elected invention, there being no allowable generic or linking claim. Election was made **without** traverse in Paper No. 10.

Drawings

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: 628, 629, 632, 699, 698, 675, 674, 697, 1032, 1033, 1250, 1252, 1221, 3040. Correction is required.

3. Fig. 26C is objected to. In Fig. 26C, 3205 and 3204 are improperly delineated.

4. Fig. 14C is objected to. In Fig. 14C, the n-channel TFT depicted contradicts the sentence bridging pages 40-41 of the specification, particularly the last line on page 4 comprising the word "overlap" since all of the LDD is "outside the gate electrode" and does not "overlap".

5. Fig. 14D is objected for showing a confusing n-channel TFT that has a skewed LDD region. Is this LDD "inside" or "outside" the "gate electrode"? The examiner interprets 206 to be "inside the gate electrode".

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1, 9, 18, 27, 36 and 81-85 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art (AAPA) in view of Hatano et al. (IEEE article).

AAPA sets forth the previous existence of driver and pixel circuitry having LDD structures "outside the gate electrode" all on the same substrate wherein there are different demands, electrically, placed on the various circuits [pages 1-6 of specification].

The independent claims cite up to five different transistors wherein p-type and n-type transistors constitute driver CMOS having GOLD (gate overlapped LDD) structures, and the pixel circuits constitute only one conductivity type transistor in the actual pixel area, these having ordinary LDD.

The examiner refrains from using the "first, second, third, fourth, and fifth transistor" language as well as the "a conductivity type" and "an opposite conductivity type" language as these are more difficult to follow.

It has long been well known that there are two types of semiconductor conductivity known as p-type and n-type, together forming CMOS, the driver circuitry explained by AAPA. There are many transistors requiring different characteristics. Particularly, the higher-speed peripheral driver circuits are limiting when they cannot scan as fast as needed, for example.

Hatano et al. recognize the need for a GOLD (gate overlapped LDD) process in TFTs that form a "system-in-display", where the driver CMOS and pixel circuitry is on the same insulating substrate [Introduction].

It would have been obvious for one of ordinary skill in the art to modify the structure of AAPA to include the Sa-GOLD TFTs taught by Hatano et al.. One of ordinary skill in the art would be motivated to include these in the higher voltage and higher speed driver circuits of the AAPA, at the suggestion of Hatano et al., to attain "high immunity against hot-carrier stress" [Conclusion].

Regarding claims 8, 17, 26, 35 and 44, it is obvious for anyone of ordinary skill in the art that a display is useful in a wide range of consumer products enumerated as "limitations". The examiner emphasizes that it is not at all surprising to apply TFT displays to consumer products because consumers demand the types of products enumerated by these claims.

8. Claims 2, 10-11, 19-20, 28-29 and 37-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Hatano et al. as applied to claims 1, 9, 18, 27 and 36 above, and further in view of Mimura et al. (U.S. 6,127,210).

Mimura et al. teach a method of forming CMOS TFT circuitry that involves dopant "compensation" as a way to reduce the number of masking steps required. As a result, the device regions having impurities for LDD and source/drain structures contain both n-type and p-type dopant, with the greater concentration setting the dopant type, the dopant type being either "n-type or p-type" (or "intrinsic" when n and p are equal).

It would have been obvious to adopt the method of Mimura et al. in using dopant "compensation" to result in a structure having both minority and majority dopant.

9. Claims 3-4, 12-13, 21-22, 30-31, 39-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Hatano et al. as applied to claims 1, 9, 18, 27 and 36 above, and further in view of Mikoshiba (U.S. 5,499,123).

Mikoshiba teaches a light-shielding layer 312 with oxidization to form insulating layer 314 on the light shield with overlap of the pixel electrode308 defining a capacitance. Mikoshiba teaches at least aluminum with aluminum oxide and tantalum with tantalum oxide.

It would have been obvious to adopt the method of Mikoshiba to get a good capacitor for the pixel. The oxidized light-shielding layer offers a good dielectric, as explained by Mikoshiba as a motivation for using his invention.

10. Claims 5-7, 14-16, 23-25, 32-34 and 41-43 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Hatano et al. taken with Mikoshiba, as applied to claims 3, 12, 21, 30 and 39 above, and further in view of Fukunaga et al. (U.S. 5,706,064).

Fukunaga et al. teach the benefits of an organic-inorganic hybrid glass layer at the capacitor dielectric in a TFT display, motivating one of ordinary skill in the art to implement the obvious improvement of using a laminate of organic and inorganic layers for increased reliability [Summary of Invention].

11. Claims 81-85 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Hatano et al. as applied to claim1, 9, 18, 27 and 36 above, and further in view of Stewart.

Stewart teaches TFT EL displays. It would have been obvious to incorporate the GOLD process taught by Hatano et al. to make EL displays because the driver circuitry in EL displays must also be higher than the pixel circuitry, in making a "system--in-display" at the suggestion of Hatano.

Conclusion

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Evan T. Pert whose telephone number is 703-306-5689. The examiner can normally be reached on M-F (7:00-3:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Charles Bowers can be reached on 703-308-2417. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Fukunaga et al. teach the benefits of an organic-inorganic hybrid glass layer at the capacitor dielectric in a TFT display, motivating one of ordinary skill in the art to implement the obvious improvement of using a laminate of organic and inorganic layers for increased reliability [Summary of Invention].

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ETP
September 10, 2001

Charles Bowers
Supervisory Patent Examiner
Technology Center 2800